Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing reply, claims 1-18 are pending in this application, with 1, 8, and 15 being the independent claims. Applicant acknowledges and thanks Examiner Nguyen for indicating claims 1-14 as allowable.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 15-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,297,162 to Jang *et al.* ("the Jang patent") in view of U.S. Patent 6,225,207 to Parikh ("the Parikh patent"). The Office Action states that: "It would of been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Parikh with the method of Jang *et al.* in order to provide for a cost effective, improved technique for damascene fabrication (col. 2, lines 50-55)." Applicant respectfully disagrees and traverses this rejection.

The Jang patent appears to teach a method to reduce silicon oxynitride etch rate in a silicon oxide dry etch. The Jang method makes use of the plasma etching process applied to forming etch stopping silicon oxynitride spacers for MOS transistors and for forming etch stopping silicon oxynitride for dual damascene interconnects. Jang does not teach or suggest that this method is applicable to MOS capacitors.

The Parick patent appears to teach a damascene process employed to fabricate structures comprising several dielectric layers and several stop etch layers. The Parick method makes use of the chemical etching process applied to forming triple and quadruple damascene integrated structures. Parick does not teach or suggest application of this method to MOS capacitors.

There is no teaching in either cited patent that indicates a combination of the two would be desirable. As such, a combination of the two can not be used, under the provisions of 35 U.S.C. § 103 to establish a prima facie case of obviousness. Specifically, Applicant asserts that the patents can't be combined in the manner suggested by the examiner because they are non-analogous art.

Plasma etching and chemical etching are two known but distinct processes used in semiconductor devices manufacturing. It is not obvious to pick method steps used by these fundamentally different etching techniques in a dual damascene process to form a MOS capacitor structure as claimed. It is improper for the Examiner to pick and chose ***structures*** disclosed by the figures of the first patent and conclude that it would of been obvious to arrive at the claimed ***method***. The Office Action cites no proper motivation to arrive at the combination of steps recited in claim 15.

Independent claim 15 discloses a process of manufacturing a metal-insulator-metal capacitor, forming its main components: the lower plate, the upper plate and the insulator.

The Office Action states that:

> Jang and Parikh fails to explicitly teach that the first metal layer is utilized as the lower plate, the etch stop layer is utilized as the insulator and the second metal layer is utilized as the upper plate of the MIM capacitor. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Parikh teaching's into Jang method to form a MIM capacitor comprises the lower plate, insulator, and upper plate in order to provide for a cost effective, improved technique for a damascene fabrication (Parikh, col. 2, lines 50-55).

Applicant agrees that there is no teaching in either cited patent that refers to a metal-insulator-metal capacitor as a whole, or its component elements: the lower plate, the insulator and the upper plate. Moreover, there is no teaching in either cited patent directed to a method, and its respective steps, of forming a metal-insulator-metal capacitor. Due to the absence of these concepts from both cited patents, Applicant disagrees with the conclusion reached in the Office Action.

The Jang and Parikh patents, either in combination or individually, fail to teach or suggest the following steps of claim 15:

> forming a first metal layer on a substrate, <u>wherein a portion of the first metal layer is utilized as the lower plate of the MIM capacitor</u>...
> [and]
> forming a second metal layer on the substrate and portion of an etch stop layer, <u>wherein a portion of the second metal layer is utilized as the upper plate of the MIM capacitor</u>...(Emphasis added.)

Therefore, Applicant respectfully submits that claim 15 is patentable over the art of record.

Applicant respectfully requests that the rejection of claim 15 be withdrawn. Further, claims 16 through 18, which depend from and add features to claim 15, are also patent able over the art of record for at least the same reasons provided above. Accordingly, reconsideration and allowance of claims 15 - 18 are requested.

Allowed subject matters

The Examiner's indication that claims 1-14 are allowed is gratefully acknowledged.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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